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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/089,137	07/08/2002	Bruce R Parnas	ADVA214.001AUS	2524

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/089,137	PARNAS, BRUCE R	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are pending and are hereby presented for examination, in response to the preset Application filed 7/8/2002.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Testa et al. (US 5845234).

Regarding independent Claim 1 and dependent claim 2, Testa discloses a method for generating testing program code for use in automatic test equipment by translating a waveform description into a unified ATE format and by taking the unified ATE format and supplying the data in a simple iterative fashion for completing templates of test program modules (Summary of the Invention), comprising:

Generating testing program code for use in automatic test equipment including converting waveforms into an ATE testing program. According to Testa, FIG. 2 is a block diagram of a prior art method for generating the testing program code 12 for use in the automatic test equipment 11. "The cyclized

waveform data 22 is converted into an ATE testing program code 24 containing format and timing information for use in a wide variety of ATE implementations" (col. 4, lines 44-56, Testa).

"Cyclized waveform data 22 is provided as program inputs. Generally, the cyclized waveform data 22 consist of waveform-based pattern data associated with waveform templates. Each set of pattern data is defined for a number of events or signals. Each waveform template defines a reusable time slice, which can be associated with multiple data pattern rows. Time slices are commonly referred to as "cycles." In essence, each waveform template describes what a set of electrical signals dc) at specific times relative to the start of a cycle. Specifications are designated for each waveform template and are usually defined for, but not limited to, a series of edge times associated with specific events. Examples of events include driving a specific logic level, turning off a driver, sampling data, driving a logic level specified by the pattern data associated with the cycle or other related functions" (col. 4, lines 19-35, Testa).

Testa discloses in FIG. 4, a data structure for storing the cyclized waveform data 22 used in the method of FIG. 3. The cyclized waveform data 22 is expressed in a waveform description language as is known in the art. The cyclized waveform data 22 stores cyclized data 40, pattern information 41 and ATE channel and device-under-test (DUT) pin information 42 as described in the following sections (col. 5, lines 29-36, Testa).

Testa describes, "The cyclized data 40 is stored according to a standard syntax for describing the waveform event data and pattern information. The

standard syntax is based on a modified STIL character set as shown below in Table 1 " which include: "E" Compare Edge Strobe to Pattern Value, "W" Compare Window Strobe to Pattern Value, "R" Compare Strobe to Inverse Pattern Value, T Compare Tristate (col. 5, lines 38-58, Testa).

Regarding independent Claim 8, Testa discloses the additional limitations. STIL is a cycle based test language with all the properties of the cycle-based waveforms in Testa. Converting STIL waveforms to ATE testing code is encompassed by Testa's invention since Testa discloses converting cycle based waveforms to ATE testing code and as such converting STIL waveforms to ATE testing code does not depart from the intended scope of Testa's invention.

Regarding Claim 5, Testa discloses, "The cyclized data 40 is stored according to a standard syntax for describing the waveform event data and pattern information. The standard syntax is based on a modified STIL character set as shown below in Table I" which include: "E" Compare Edge Strobe to Pattern Value, "W" Compare Window Strobe to Pattern Value, "R" Compare Strobe to Inverse Pattern Value, "T" Compare Tristate (col. 5, lines 38-58, Testa). Testa discloses, "data is in a form that allows simple mapping of the information into list driven templates for generating the output ATE test program modules (col. 11, lines 51-65, Testa).

Regarding Claim 6, Testa discloses "each waveform template describes what a set of electrical signals do at specific times relative to the start of a cycle" and "waveform template and are usually defined for but not limited to, a series of edge times associated with specific events" (cot. 4, lines 19-35, Testa).

Regarding Claim 7, Testa discloses " the signals can be grouped into higher level constructs which include: (I) buses 49A-C; and (2) multiplexed groups 50A-C. Each bus 49A is an indexed list of signals all associated with one name Each multiplexed group 50A is a grouping of two or more signals which are grouped together to show combined signal information (col. 7, lines 5-10, Testa).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Testa et al. (US 5845234).

Testa substantially discloses the claimed invention as applied with respect to independent claim, above.

Regarding Claims 3, 4 Testa does not teach the step of storing test data in a table consisting of start time and subsequent edges. Testa discloses "each waveform template describes what a set of electrical signals do at specific times relative to the start of a cycle" and "waveform template and are usually defined for, but not limited to, a series of edge times associated with specific events" (col. 4, lines 19-35, Testa). Testa further discloses in FIG. 4, " a data structure for

storing the cyclized waveform" (col. 5, lines 29-36, Testa). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include an additional step of storing test data in a table consisting of start time and subsequent edges in the method of Testa. One of ordinary skill in the art would have been motivated to do this modification, since storing test data in a table consisting of start time and subsequent edges would eventually enhance testing.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reichert (US 6553529) discloses a high-speed test waveform suitable for application to a DUT defined by timing signals generated by the timing system FIG. 3. Each transition (or "edge") of the test waveform corresponds to the output of a driver responding to timing signals issued by the edge generators EG0-EG12. FIG. 4 shows an edge-set memory 36 corresponding to the test waveform of FIG. 3 including a table for inserting desired timing values for the timing generators to define the waveform transitions, or edges corresponding to the above events (D0, D1, strobe, Vt).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

By:

Examiner's Fax: (703) 746-4461

Date: 16 August 2004
Office Action: Non-Final Rejection

James C Kerveros
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100